



Jumper JP1 allows selection of CAS or a "delayed" CAS
 OE of the 128Kx8 SRAM tied to GND allows WE to act as R/W
 RAS strobes the first half of the address into the latch.
 CAS strobes both halves of the address into the SRAM
 A16 is tied high since only half of the 128Kx8 SRAM is used
 WE then allows: a read of the SRAM if high, otherwise data is written into the SRAM
 Note that CAS strobes the CS1 line which enables the SRAM for the duration of CAS only
 CS2 is tied high and must remain high in order that the SRAM may be enabled
 A16, shown tied high, can be high or low - it doesn't matter which half of the SRAM we use
 A16 could also be attached to an S-R flip-flop to provide a bank switching circuit,
 thus providing two 64K Banks of RAM
 Note that the SRAM is the LP (Low Power) version, which also allows for a battery backup circuit to be used
 THIS CIRCUIT HAS PROVEN SUCCESSFUL AT REPLACING A BANK OF EIGHT 4164 DRAMS
 NOTE, HOWEVER, THAT THIS CIRCUIT ASSUMES THAT THE DO & DI OF THE DRAMS
 ARE TIED TOGETHER. THIS IS NOT ALWAYS THE CASE - THE CoCo 2, FOR EXAMPLE
 DOES NOT HAVE THE DO & DI PINS OF THE DRAM TIED TOGETHER. IN SUCH A CASE
 A SET OF TRI-STATE BUFFERS MUST BE INCORPORATED ON THE SRAM DATA BUS PINS
 SEE: 4164 DRAM - SRAM Replacement #2 for the circuit to use in such an instance.