



4164 DRAM - SRAM Replacement #2, by: J&R of GIMEchip.com, (c)9 JUNE 2010

Jumper JP1 allows selection of $\overline{\text{CAS}}$ or a "delayed" $\overline{\text{CAS}}$.
 $\overline{\text{OE}}$ of the 128Kx8 SRAM tied to GND allows $\overline{\text{WE}}$ to act as R/W.
 $\overline{\text{RAS}}$ strobes the first half of the address into the latch.
 $\overline{\text{CAS}}$ strobes both halves of the address into the SRAM.
A16 is tied high since only half of the 128Kx8 SRAM is used.
 $\overline{\text{WE}}$ then allows: a read of the SRAM if high, otherwise data is written into the SRAM.
Note that $\overline{\text{CAS}}$ strobes the $\overline{\text{CS1}}$ line which enables the SRAM for the duration of $\overline{\text{CAS}}$ only.
CS2 is tied high and must remain high in order that the SRAM may be enabled.
A16, shown tied high, can be high or low - it doesn't matter which half of the SRAM we use.
A16 could also be attached to an S-R flip-flop to provide a bank switching circuit, thus providing two 64K Banks of RAM.
Note that the SRAM is the LP (Low Power) version, which also allows for a battery backup circuit to be used.
THIS CIRCUIT HAS PROVEN SUCCESSFUL AT REPLACING A BANK OF EIGHT 4164 DRAMS.
NOTE, HOWEVER, THAT THIS CIRCUIT ASSUMES THAT THE DO & DI OF THE DRAMS
ARE USED SEPERATELY BY THE TARGET CIRCUIT. THIS MAY NOT ALWAYS BE THE CASE, AS
SOME DESIGNS SIMPLY TIE THE DO & DI PINS TOGETHER. IT DOESN'T MATTER TO THIS CIRCUIT WHETHER THE
DO & DI PINS ARE TIED TOGETHER OR NOT. IT WILL WORK REGARDLESS. HOWEVER, IF THE TARGET CIRCUIT
HAS THE DO & DI PINS TIED TOGETHER, THEN THIS CIRCUIT CAN BE SIMPLIFIED BY LEAVING OUT THE DO & DI
BUFFERS. THE SIMPLIFIED CIRCUIT FOR SUCH AN INSTANCE IS PROVIDED IN THE FIRST PART OF THIS SERIES:
SEE: 4164 DRAM - SRAM Replacement #1 for the circuit to use when DO & DI are tied together.

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